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CSE 310

Homework 2

1. Consider a 2s complement 8-bit representation. A binary number has a value of 103 when we regard it as a signed number. What is its value if we regard it as an unsigned number?

The value of 103 when regarded as a unsigned number is 152 since unsigned numbers have a range of 255 to 0 so to get the unsigned number we do 255 – 103 which equals to 152.

1. Consider a 2s complement 8-bit representation. What is the value of 0001 1010?

0001 1010 = (0 × 2⁷) + (0 × 2⁶) + (0 × 2⁵) + (1 × 2⁴) + (1 × 2³) + (0 × 2²) + (1 × 2¹) + (0 × 2⁰) = 16 + 8 + 4 + 2 = 26

1. Simply the boolean expression x' + xy + xz' +xy'z'. What is the simplest result?
2. Simplify (x + y)'(x' + y'). What is the simplest result?
3. Simplify x \* ( x + y + z ) \* ( x' + y ) \* ( x + q ) \* ( x + q' + z ).
4. Simplify x \* ( x + y + z' ) \* ( x' + z ) \* ( y + z' ) \* ( x + z )

1. Write the boolean expression (in sum-of-product form) for a logic circuit that will have a 1 output when x = 0, y = 0, z = 1 and x = 1, y = 1, z = 0; and a 0 output for all other input states. Draw the circuit for the simplified expression.

X = 0, Y = 0, Z = 1

|  |  |  |  |
| --- | --- | --- | --- |
| X | Y | Z | F |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 |

Circuit Diagram

X

Y

Z

* X = 1, Y = 1, Z = 0

|  |  |  |  |
| --- | --- | --- | --- |
| X | Y | Z | F |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |

Circuit Diagram

Same as the one above

1. Simplify the expression xyz (xyz' + xy'z + x'yz ).

1. Using maps or whatever method you prefer, simplify the following expressions in four variables, w, x, y and z:

http://cse.csusb.edu/tongyu/courses/images/sum.png ( 0,2,4,8,9,10,11,12,13)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | wx |  |  |  |  |
| yz |  | 00 | 01 | 11 | 10 |
|  | 00 | 1 | 0 | 0 | 1 |
|  | 01 | 1 | 0 | 0 | 0 |
|  | 11 | 1 | 1 | 0 | 0 |
|  | 10 | 1 | 1 | 1 | 1 |

1. Write Verilog modules and a test bench to check whether your simplified expressions of question 5 and 6 are correct. Use both the structural description and behavioral description.

*hwk2.v*

// x \* ( x + y + z ) \* ( x' + y ) \* ( x + q ) \* ( x + q' + z ).

module Problem5 ( output F, input x, input y, input z, input q );

assign F = x && ( x || y || z ) && ( !x || y ) && ( x || q ) && ( x || !q || z );

endmodule

// x \* ( x' + y )

module Problem5\_Solution ( output F, input x, input y );

assign F = x && ( !x || y );

endmodule

// x \* ( x + y + z' ) \* ( x' + z ) \* ( y + z' ) \* ( x + z )

module Problem6 ( output F, input x, input y, input z );

assign F = x && ( x || y || !z ) && ( !x || z ) && ( y || !z ) && ( x || z );

endmodule

// x \* y \* z

module Problem6\_Solution ( output F, input x, input y, input z );

assign F = x && y && z;

endmodule

*hwk2\_tb.v*

module testBench();

reg x, y, z, q;

wire F1, F2;

// Intialize all variables

initial begin

$display ("time\t x y z q F1 F2");

$monitor ("%g\t %b %b %b %b %b %b",

$time, x, y, z, q, F1, F2);

x = 0;

y = 0;

z = 0;

q = 0;

#75 $finish;

end

always begin

#5 q = ~q;

end

always begin

#10 z = ~z;

end

always begin

#20 y = ~y;

end

always begin

#40 x = ~x;

end

// Problem5 test1 ( .F(F1), .x(x), .y(y), .z(z), .q(q) );

// Problem5\_Solution test1Sol ( .F(F2), .x(x), .y(y) );

Problem6 test2 ( .F(F1), .x(x), .y(y), .z(z) );

Problem6\_Solution test2Sol ( .F(F2), .x(x), .y(y), .z(z) );

endmodule

Outputs:

* Problem 5

**georgesuarez at MacBook-Pro in ~/University/cse310/Homework/Homework 2 on master\***

**$** ./hwk2\_tb

time x y z q F1 F2

0 0 0 0 0 0 0

5 0 0 0 1 0 0

10 0 0 1 0 0 0

15 0 0 1 1 0 0

20 0 1 0 0 0 0

25 0 1 0 1 0 0

30 0 1 1 0 0 0

35 0 1 1 1 0 0

40 1 0 0 0 0 0

45 1 0 0 1 0 0

50 1 0 1 0 0 0

55 1 0 1 1 0 0

60 1 1 0 0 1 1

65 1 1 0 1 1 1

70 1 1 1 0 1 1

75 1 1 1 1 1 1

~

* Problem 6

**georgesuarez at MacBook-Pro in ~/University/cse310/Homework/Homework 2 on master\***

**$** ./hwk2\_tb

time x y z q F1 F2

0 0 0 0 0 0 0

5 0 0 0 1 0 0

10 0 0 1 0 0 0

15 0 0 1 1 0 0

20 0 1 0 0 0 0

25 0 1 0 1 0 0

30 0 1 1 0 0 0

35 0 1 1 1 0 0

40 1 0 0 0 0 0

45 1 0 0 1 0 0

50 1 0 1 0 0 0

55 1 0 1 1 0 0

60 1 1 0 0 0 0

65 1 1 0 1 0 0

70 1 1 1 0 1 1

75 1 1 1 1 1 1